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(54) **Circuit for PCM conversion of an analogic signal, with improvement in gain-tracking.**

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(56) References cited:

1986 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE, New York, 20th February 1986, pages 180-181, IEEE, New York, US; K. YAMAKIDO et al.: "A voiceband 15b interpolative converter chip set"

IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-15, no. 6, December 1980, pages 1014-1021, IEEE, New York, US; H. KUWAHARA et al.: "An interpolative PCM CODEC with multiplexed digital filters"

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ELECTRONIC COMPONENTS & APPL., vol. 2,
no. 4, August 1980, pages 242-250, Eind-
hoven, NL; D.J.G. JANSSEN et al.: "PCM
codec with on-chip digital filters"

1987 IEEE INTERNATIONAL SYMPOSIUM ON
CIRCUITS AND SYSTEMS, Philadelphia, PA,
4th-7th May 1987, pages 467-472, IEEE, New
York, US; A. YUKAWA: "Constraints analysis
for oversampling A-to-D converter struc-
tures on VLSI implementation"

Description

The present invention relates to a circuit for PCM conversion of an analogic signal, such as a voice signal, with improvement of gain-tracking.

In recent years PCM (Pulse Code Modulation) coding has become very widespread, until it has become the modulation method most used in telephone systems. Among the various international recommendations (such as CCITT in Europe) which set rules on every possible telephone connection, those related to the PCM converter (normally constituted by an integrated circuit known as "Combochip") prescribe, among other things, a mask (described hereinafter) for limiting the gain error (i.e. gain-tracking) as the level of the input signal, assumed sinusoidal, varies.

Analogic-digital conversion is performed with a quantizer which forces the analogic signal to assume only preset discrete values, and with a sampler which samples the quantized signal and feeds the successive samples to an encoder. Since analogic-digital conversion introduces, as is known, a quantization error in the signal to be encoded, this reflects in a corresponding error in the encoded signal, equivalent to a gain error, even for an ideal "combochip".

The aim of the invention is now to provide a PCM conversion circuit ("combochip") having a gain-tracking better than that of known circuits, and actually better than the one considered ideal.

The invention achieves the above described aim, as well as other objects and advantages which will become apparent hereinafter, with a circuit for PCM conversion of an analog circuit, as defined by claim 1.

The invention is now described in greater detail with reference to a preferred embodiment thereof, illustrated in the accompanying drawings, wherein:

figure 1 is a diagram illustrating a mask for limiting the gain error and the ideal gain-tracking, according to the prior art;

figure 2 is a block diagram of a PCM conversion circuit according to the prior art;

figure 3 is a block diagram of a preferred embodiment of PCM conversion circuit according to the invention;

figure 4 is a diagram illustrating the gain-tracking obtained with the circuit of figure 3; and

figure 5 is an example of practical execution of the conversion circuit of figure 3.

In figure 1, which is a diagram of the variation in gain in dB as a function of the input signal level, also in dB, the two broken lines define a mask within which, according to CCITT recommendations, the gain variation curve must be comprised. The mask is referred to the gain at -10 dBm0, i.e. it assumes that the gain is measured when the

sinusoidal input signal is equal to -10 dBm0 as absolute reference.

Figure 2 illustrates a PCM conversion circuit according to the prior art. It comprises a high-pass filter 10 which receives an analogic input signal V_{in} , typically a voice signal. It is supposed that the signal V_{in} has been previously filtered in a low-pass filter, not illustrated, with cutoff frequency lower than half the sampling frequency f_s , according to criteria known to the experts in the field. The output signal V_{out} of the high-pass filter 10 enters a PCM converter 11 comprising a quantizer 12, known to the expert in the field, which produces an output signal V_Q in steps, forced to assume values in a discrete series, a sampler 14, which receives the output signal V_Q of the quantizer and samples it at a desired frequency f_s , typically 8 kHz, to generate a quantized sampled signal V_{QS} , and an encoder 16, which encodes the signal V_{QS} in PCM pulses.

PCM encoders typically operate by successive comparisons of the sample of signal with gradually more proximate references, and in general at the end of the conversion there is available, on an adder node of the circuit, the residual difference, or remainder, between the sample and the reference. An example of PCM encoder of this type is described for example in the article "A Segmented μ -255 Law PCM Voice Encoder Utilizing NMOS Technology", by Yannis P. Tsvidis et al., in *IEEE J. Solid-State Circuits*, vol. SC-11, pp. 740-747, Dec. 1976.

According to the invention, as illustrated in figure 3, the PCM conversion circuit comprises, besides the stages 10, 12, 14 and 16 of figure 2, a remainder feedback circuit 18, connected to receive said residual difference from the adder node 20 of the PCM converter and inject it, with or without further processing such as appropriate filtering, in a stage of the high-pass filter 10 such that the overall transfer function from the input of the remainder feedback circuit 18 to the output of the high-pass filter 10 is equivalent to a low-pass filtering.

With the circuit arrangement described above with reference to figure 3, a gain-tracking as illustrated in figure 4 is obtained, having the same meaning of figure 1. As is apparent, the gain-tracking is improved with respect to the one considered ideal illustrated in figure 1.

Though the inventors do not have a full understanding of the theoretical reasons for this result, the feedback of the remainder seems to have the effect of distributing more uniformly the quantization error, eliminating the error peaks which occur at the transitions of the signal from a discrete quantization level to another.

Figure 5 illustrates a more specific example of the invention. The high-pass filter 10 of figure 3 has

an input terminal IN and an output terminal OUT, and is provided with three operational amplifiers 30, 32 and 34, interconnected in a known manner with coupling and integration capacitors 36, and with switched capacitors 38. The remainder feedback circuit 18 is provided as a simple switched capacitor 40, which alternately charges from the adder node 20 of the PCM converter 11 and discharges onto the input of the third operational amplifier 34 of the filter 10. It can be seen that the transfer function from the adder node 20 to the OUT terminal of the filter corresponds to a low-pass filtering.

The remainder feedback circuit 18, instead of being provided with a simple switched capacitor, may also be a complex network, such as to impart to the signal a different filtering, and the feedback of the remainder may be executed in another stage of the filter, for example at the input.

Preferred embodiments of the invention have been described, but it is understood that the scope of the invention is limited only by the appended claims.

Where technical features mentioned in any claim are followed by reference signs, those reference signs have been included just for the sole purpose of increasing intelligibility of the claims and accordingly, such reference signs do not have any limiting effect on the scope of each element identified by way of example by such reference signs.

Claims

1. Circuit for the PCM conversion of an analog signal comprising a filter (10) including several stages and having an input (IN) at which the analog signal is applied, a quantizer (12) driven by the filter (10) for generating a quantized signal according to the received analog signal, a sampler (14) driven by the quantizer (12) for sampling the quantized signal at a frequency that is substantially twice the analog signal cut-off frequency, and PCM encoder (16) driven by the sampler (14), CHARACTERIZED IN THAT the quantizer means (12) further comprises circuit means for detecting a difference signal representative of the difference between the analog signal and the quantized one, feedback circuit means (18) being coupled between the circuit means and a stage of the filter (10) for feeding back the difference signal, wherein the overall transfer function from the output (20) of the circuit means to the output (OUT) of the filter (10) corresponds to a low-pass filtering.
2. Circuit according to claim 1, characterized in that the filter (10) is a high-pass filter.

3. Circuit according to either of claims 1-2, characterized in that said filter (10) comprises multiple stages (30,32, 34), and in that said feedback circuit means (18) is coupled to a later stage (34) thereof.
4. Circuit according to either of claims 1-2, characterized in that said filter (10) comprises multiple stages (30,32, 34), and in that said feedback circuit means (18) is coupled to an input stage (30) thereof.
5. Circuit according to one or more of the preceding claims, characterized in that said feedback circuit means (18) includes a switched capacitor (40).

Patentansprüche

1. Schaltung zur PCM-Wandlung eines Analogsignals, enthaltend ein Filter 10 mit mehreren Stufen und mit einem Eingang (IN), dem das Analogsignal zugeführt ist, einem Quantisierer (12), das von dem Filter (10) versorgt wird, um ein quantisiertes Signal in Übereinstimmung mit dem empfangenen Analogsignal zu erzeugen, einen Abtaster (14), der von dem Quantisierer (12) versorgt wird, um das quantisierte Signal mit einer Frequenz abzutasten, die im wesentlichen das doppelte der oberen Grenzfrequenz des Analogsignals ist, und einen PCM-Codierer (16), der von dem Abtaster (14) versorgt ist, **dadurch gekennzeichnet**, daß der Quantisierer (12) weiterhin eine Schaltung zur Ermittlung eines Differenzsignals enthält, das für die Differenz zwischen dem Analogsignal und dem quantisierten Signal repräsentativ ist, und eine Rückkopplungsschaltung (18) zwischen die genannte Schaltung und eine Stufe des Filters (10) gekoppelt ist, um das Differenzsignal rückzukoppeln, wobei die Gesamtübertragungsfunktion vom Ausgang (20) der genannten Schaltung zum Ausgang (OUT) des Filters (10) einer Tiefpaßfilterung entspricht.
2. Schaltung nach Anspruch 1, **dadurch gekennzeichnet**, daß das Filter (10) ein Hochpaßfilter ist.
3. Schaltung nach einem der Ansprüche 1 und 2, **dadurch gekennzeichnet**, daß das Filter (10) mehrere Stufen (30, 32, 34) enthält und daß die Rückkopplungsschaltung (18) mit einer späteren Stufe (34) desselben verbunden ist.
4. Schaltung nach einem der Ansprüche 1 und 2, **dadurch gekennzeichnet**, daß das Filter (10)

mehrere Stufen (30, 32, 34) enthält und daß die Rückkopplungsschaltung (18) mit einer Eingangsstufe (30) desselben verbunden ist.

5. Schaltung nach einem oder mehreren der vorhergehenden Ansprüche, **dadurch gekennzeichnet**, daß die Rückkopplungsschaltung (18) einen geschalteten Kondensator (40) enthält.

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Revendications

1. Circuit de conversion en MIC (Modulation par impulsions codées) d'un signal analogique, comprenant un filtre (10) ayant plusieurs étages et une entrée (IN) au niveau de laquelle est appliqué le signal analogique, un quantificateur (12) recevant la sortie du filtre (10) pour produire un signal quantifié en fonction du signal analogique reçu, un échantillonneur (14) recevant la sortie du quantificateur (12) pour échantillonner les signaux quantifiés à une fréquence qui est sensiblement le double de la fréquence de coupure du signal analogique, et un codeur MIC (16) recevant la sortie de l'échantillonneur (14), caractérisé en ce que le moyen quantificateur (12) comprend en outre des moyens de circuit pour détecter un signal de différence représentatif de la différence entre le signal analogique et le signal quantifié, un moyen de circuit de réaction (18) étant couplé entre les moyens de circuit et un étage du filtre (10) pour renvoyer le signal de différence, dans lequel la fonction de transfert d'ensemble, de la sortie (20) des moyens de circuit à la sortie (OUT) du filtre (10), correspond à un filtrage passe-bas.
2. Circuit selon la revendication 1, caractérisé en ce que le filtre (10) est un filtre passe-haut.
3. Circuit selon l'une des revendications 1 ou 2, caractérisé en ce que le filtre (10) comprend plusieurs étages (30, 32, 34) et en ce que le moyen de circuit de réaction (18) est couplé à un dernier étage (34) de celui-ci.
4. Circuit selon l'une des revendications 1 ou 2, caractérisé en ce que le filtre (10) comprend plusieurs étages (30, 32, 34) et en ce que le moyen de circuit de réaction (18) est couplé à un étage d'entrée (30) de celui-ci.
5. Circuit selon une ou plusieurs des revendications précédentes, caractérisé en ce que le moyen de circuit de réaction comprend une capacité commutée (40).

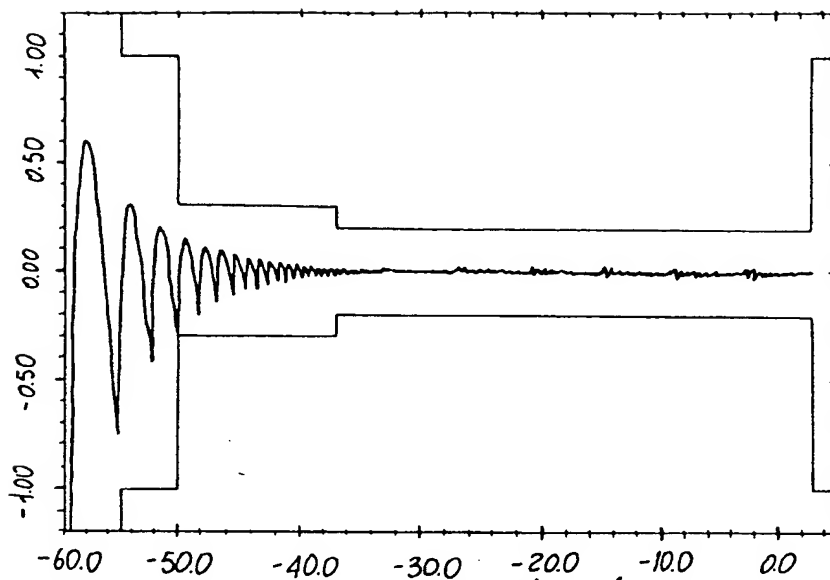


FIG. 1

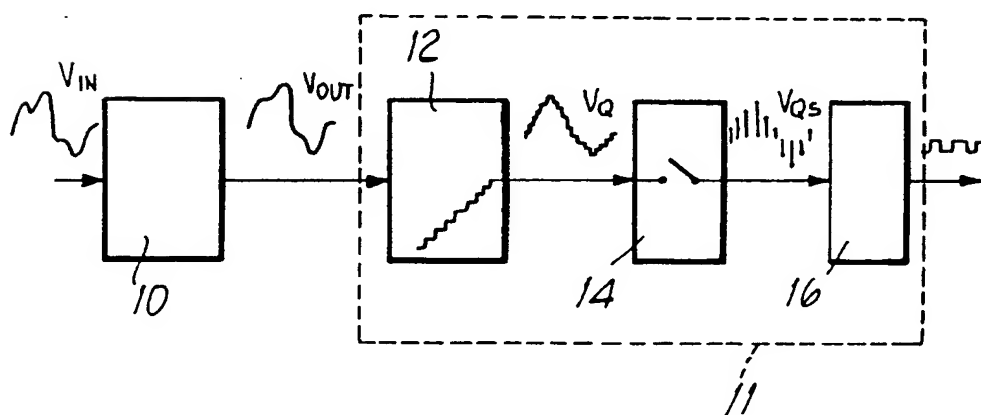


FIG. 2

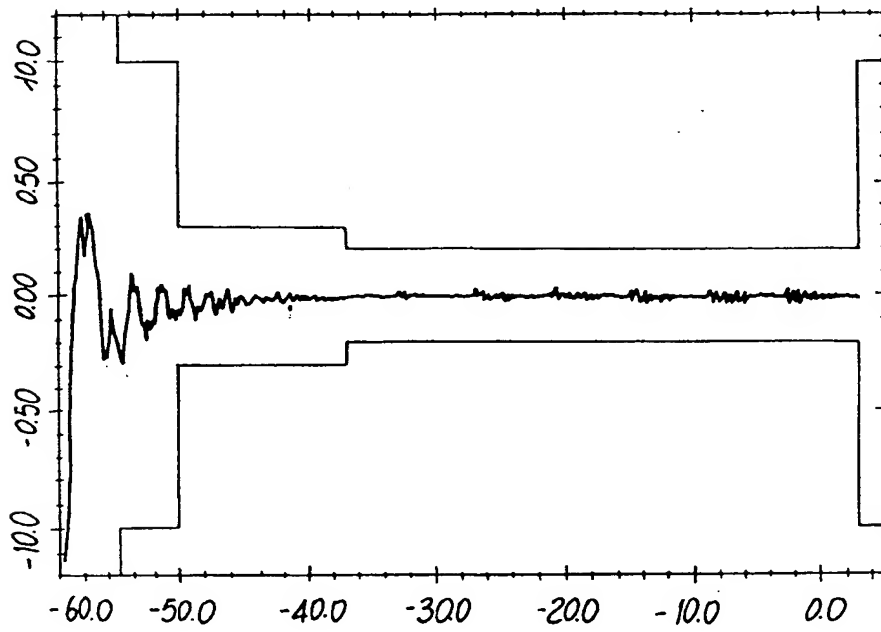
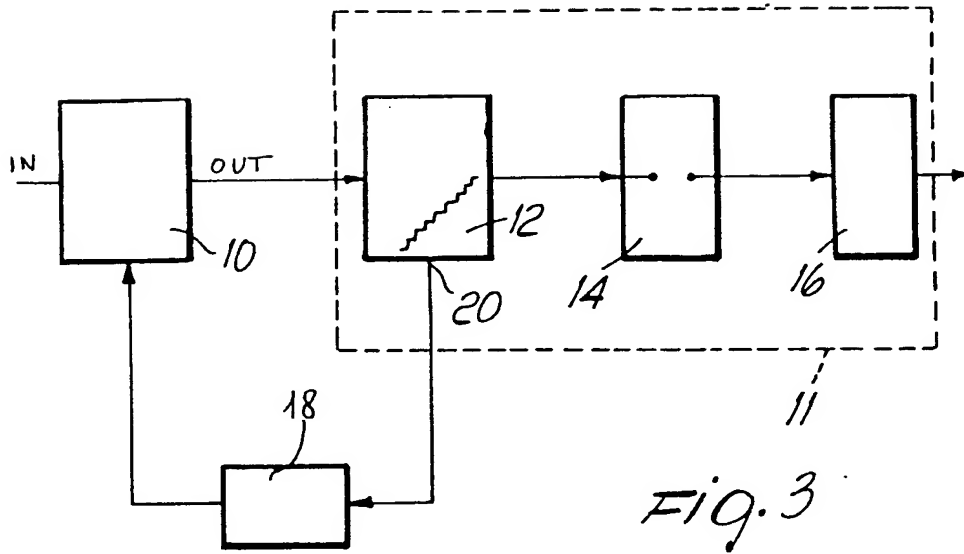


Fig. 4

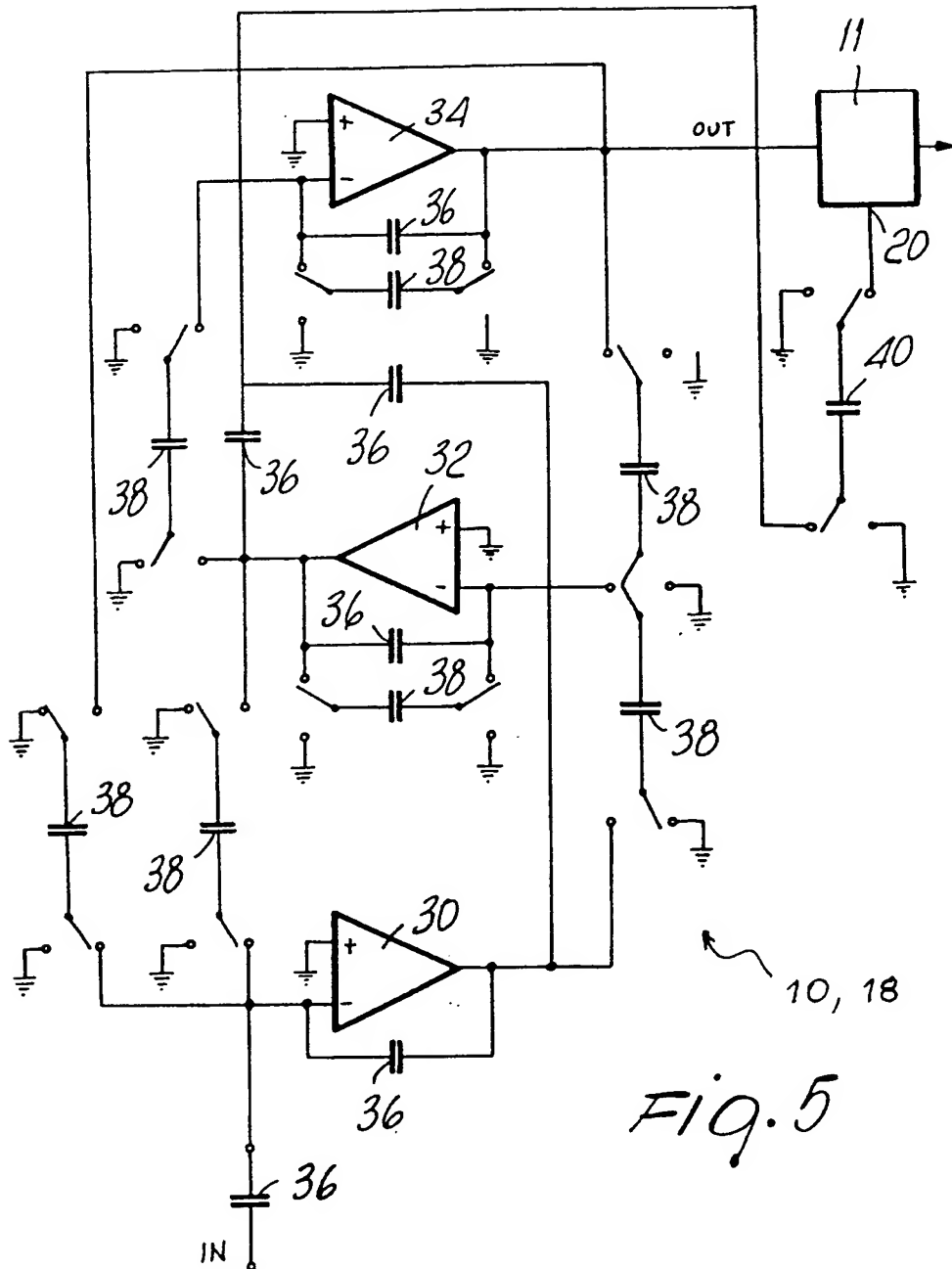


Fig. 5